CONSUMING DYNAMIC INTERCHANGING ACITIVITY OF MULTIPLIER RELATIONS OF LOW POWER VLSI DESIGN FOR RECONFIGURABLE FIR FILTER

[1] P PUSHPA, [2] T SRI LAKSHMI, [3] T SOWMYA
[1,2,3] Assistant professor, Department of Electronics and Communication Engineering,
St. Martin's Engineering College, Hyderabad-500100

Abstract: In the Internet of Things, the most widely implemented components are FIR filters with reconfigurable hardware, since they consume a minimum amount of energy to support various applications. The choice of optimal coefficients in the design of reconfigurable FIR (RFIR) filters plays an important role. The multiplier components used in these FIR filters are responsible for significant energy consumption. In this document, two multiplier topologies, one is the Baugh-Wooley (BW2) radix-2 multiplier and the other is the Booth-Recoded (BR4) radix-4 multiplier implemented in RFIR filters and has proposed a technique to analyse the 'dynamic switching activity in multipliers. The results of the dynamic power comparison show that the FIR filter implemented with the BW2 multiplier provides lower dynamic energy consumption than the FIR filter implemented with the BR4 multiplier. The FIR filter with two multiplying topologies is implemented in VHDL, the filter coefficients are generated using MATLAB and synthesized using the Xilinx synthesis tool and the ISIM simulator and the dynamic power is calculated using the cadence match.

Keywords: Baugh-Wooley multiplier, Booth Recoded Multiplier, Dynamic switching power, optimal coefficients, Reconfigurable FIR filter.

I. INTRODUCTION

Digital Signal Processing (DSP) has a great significance in many applications. Filtering is one of the extensively used operations in DSP. [1]. Finite impulse response (FIR) filters are fundamental building blocks for many DSP applications. Due to continuous operation of FIR filters, they are responsible for large power consumption in the system. So, there is a need to implement low power technique in FIR filters. Several researchers purposed many VLSI architectures for low power realization of FIR filters on programmable DSP's [2]. From the dynamic power equation, the dynamic power is quadratic dependent on supply voltage. Voltage over scaling (VOS) techniques **[**3], [4] is proposed for low dynamic power. VOS refers to scaling supply voltage beyond the limit imposed by the throughput constraints. In these, arithmetic operations are implemented using ripple carry adder (RCA) which is one of the slowest adders. What mough *et al.* [5], proposed another method for voltage over scaling based on carry merge adder and critical path delays. Multipliers are the major components in FIR filter. There are some techniques called distributed arithmetic (DA) [6], based approach for multiplier less FIR filter. Look up tables (LUT's) are used to store the coefficients of filter. Shared LUT's design is proposed by S. Y. Park and P. K. Meher [7] to realize the DA computation by sharing the registers for bit slices of different weightage. Several techniques like design of approximate multipliers for low power operation [8], [9] and low power parallel multiplier design for DSP application [10] are proposed by designing inaccurate multiplier block for large power efficient. In this paper dynamic switching power of 8-tap FIR filter with two multiplier topologies is implemented. The rest of the paper is organized as follows: Section II, Implementing VLSI architectures for FIR filters radix-2 with Baugh-Wooley multiplier and radix-4 Booth-Recoded multiplier.

Section III presents simulation results. Dynamic power comparisons are presented in section IV. Finally, section V presents conclusion.

II. RECONFIGURABLE FIR FILTER ARCHITECTURE

2.1 RADIX-2 BAUGH-WOOLEY MULTIPLIER ARCHITECTURE

I have considered two most commonly used multiplier topologies for analyzing the switching activity of the multipliers, one is radix-2 Baugh-Wooley multiplier (BW2) and the other is radix-4 Booth-Recoded multiplier (BR4). The structure of BW2 multiplier is shown in fig.1. This multiplier is a simple symmetric structure and operates with medium operating speed. In the implemented architecture two inputs X, Y of n-bits are given to the partial product generator (PPG) to implement the Baugh-Wooley scheme. The generated partial products are fed to partial product reducer (PPR) which is implemented using carry save adder (CSA) with tree structure. The tree structure in PPR is implemented using adders and the sum and carry of PPR are fed to the vector merging adder (VMA) which is implemented using carry propagate adder. The VMA provides the result of the multiplier. In this architecture I have reduced the switching activity of the multiplier by providing more no of bits equal to zero in atleast anyone of the inputs. The dynamic switching power of the multiplier is analyzed by providing a constant value to one input operand and a random value to other input operand. Due to symmetric nature of BW2 any one input can be kept constant and the other input varying.

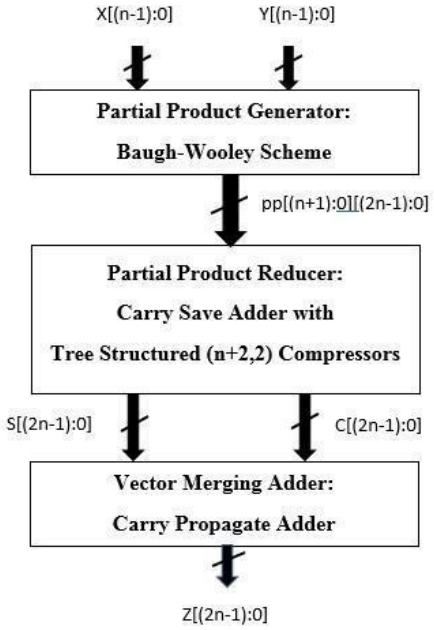


Fig.1. Structure of signed n-bit radix-2 Baugh-Wooley multiplier

2.2 RADIX-4 BOOTH RECODED ARCHITECTURE

The VLSI architecture of BR4 multiplier is shown in Fig.2. The radix-4 Booth-Recoded (BR4) multiplier is a complex asymmetric structure and operates with high speed. The PPR and VMA of BR4 multiplier is implemented same as BW2 multiplier.

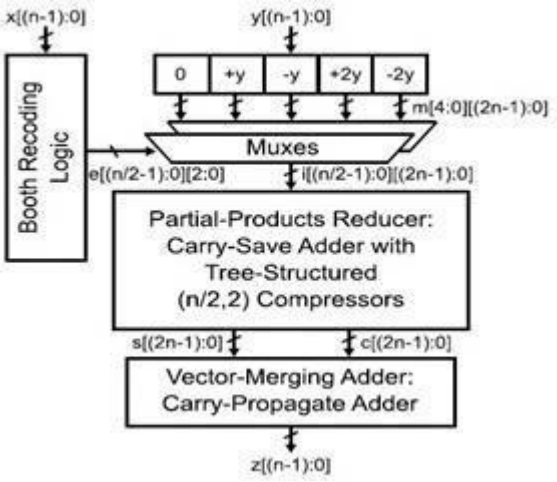


Fig.2. Structure of signed n-bit radix-4 Booth Recoded multiplier

In this structure also, the dynamic switching activity of the multiplier is analyzed by providing more no. of zeros in atleast one input. Due to asymmetric structure of BR4, the dynamic power is analyzed by providing constant input to recoding logic and random value to other input.

2.3 ARCHITECTURE OF 8-TAP RECONFIGURABLE FIR FILTER

The block diagram of 8-tap FIR filter is shown in Fig.3. The two multiplier topologies, BW2 and BR4 are implemented in 8-tap RFIR filter. The filter coefficients are kept as constant operands and the data operand of the filter is provided randomly. For different cut-off frequencies and different windowing methods the coefficients of FIR low pass filter are taken and provided as constant operands to the multipliers.

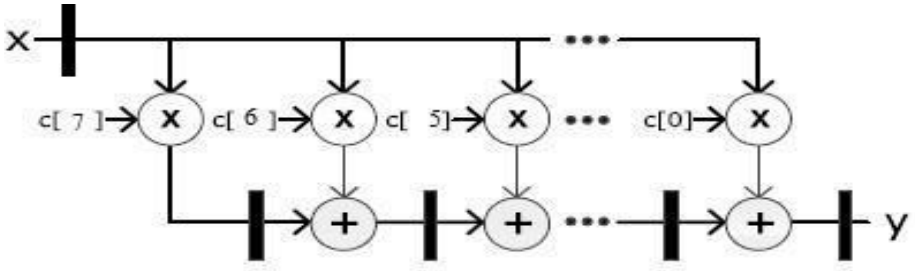


Fig.3. Structure of 8-tap FIR Filter

III. SIMULATION RESULTS

The proposed VLSI architectures for 8-bit BW2 multiplier, BR4 multiplier and 8-tap FIR filter are written in VHDL, synthesized and simulated using Xilinx and ISIM simulator.

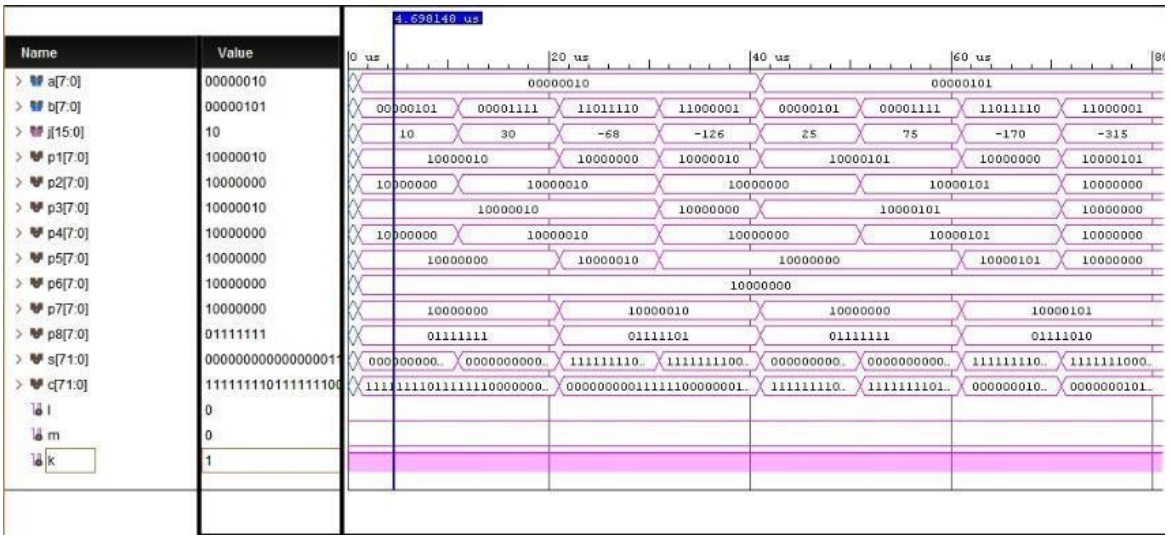


Fig.4. Simulation Result of bit BW2 multiplier

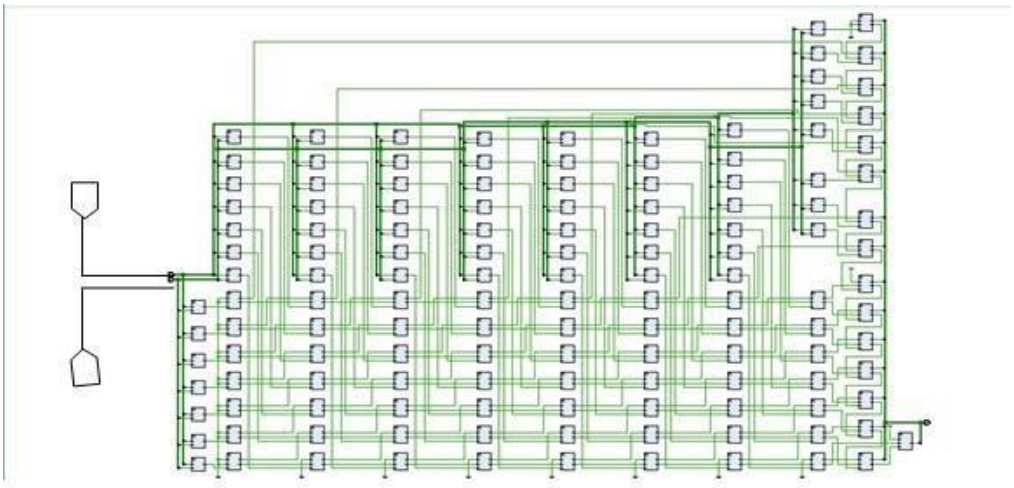


Fig.5. RTL Schematic of BW2 multiplier

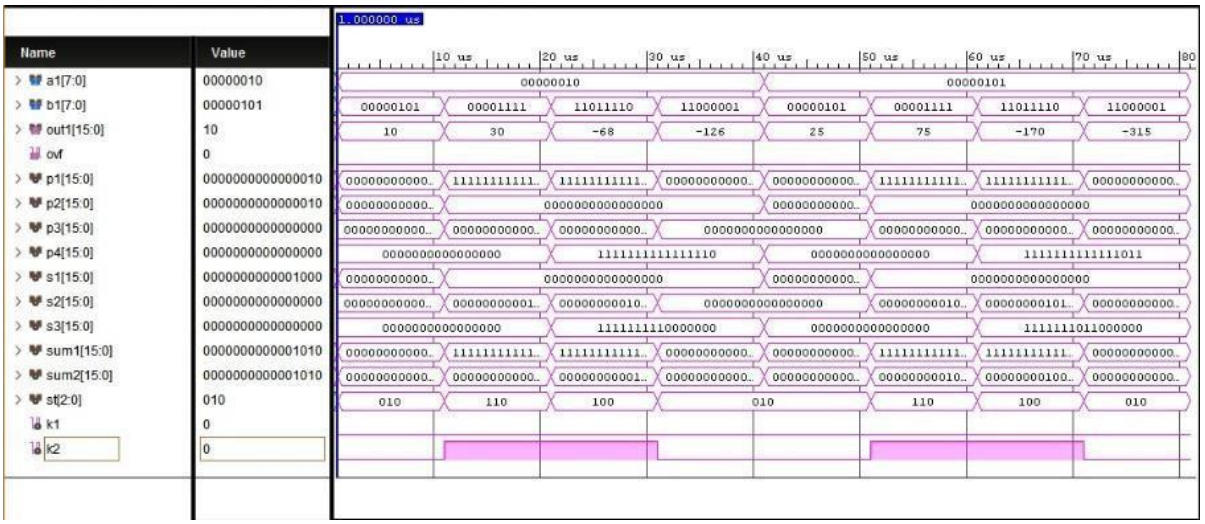


Fig.6. Simulation result of BR4 multiplier

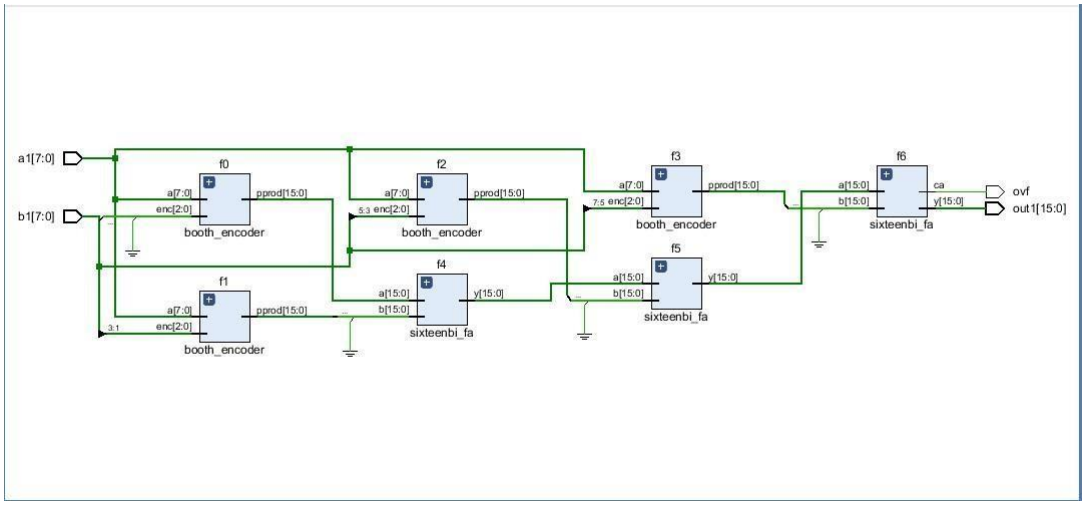
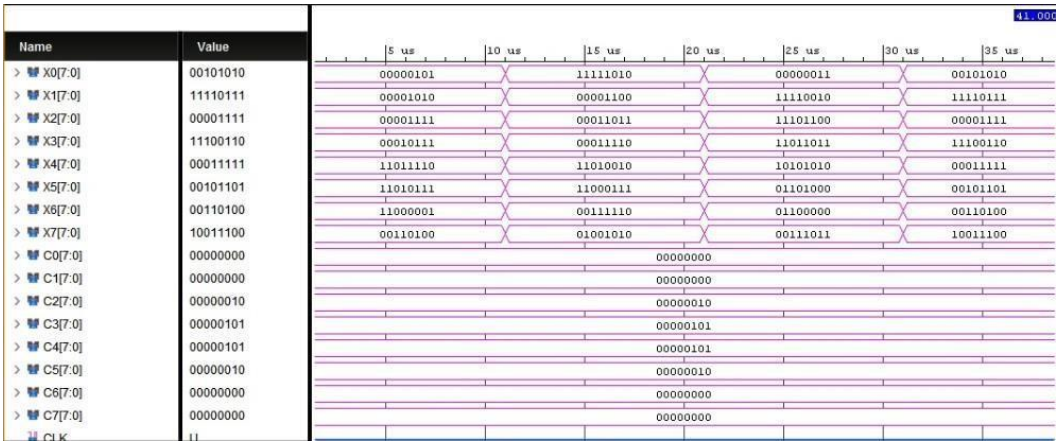


Fig.7. RTL Schematic of BR4 multiplier

The implemented VLSI architecture of FIR filter is shown in Fig:8. In this the filter coefficients are designed from MATLAB by taking a Bartlett low pass FIR filter with normalized cut-off frequency 0.35 rad/sample. In this the coefficients C0 to C1, are taken as constant operands for many clock cycles and by varying the data operands X0 to X1, the filter outputs Y0 to Y14, are observed.



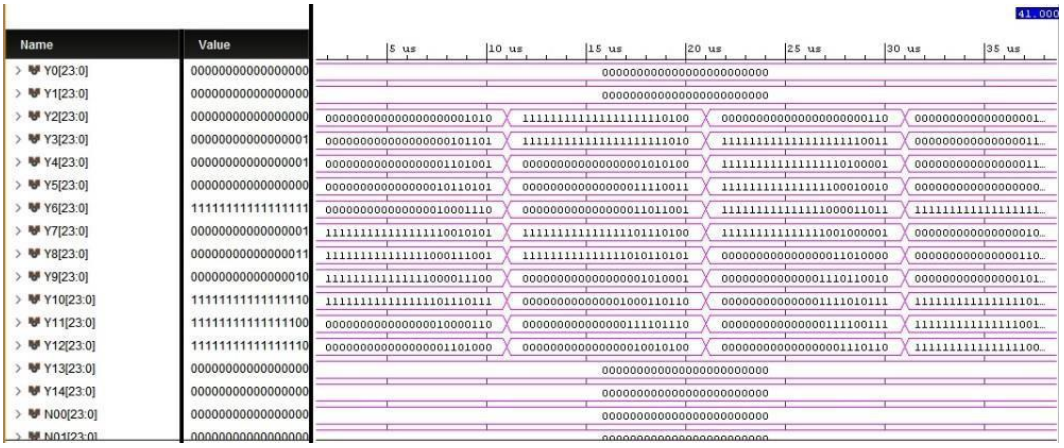


Fig.8. Simulation result of 8-tap FIR filter

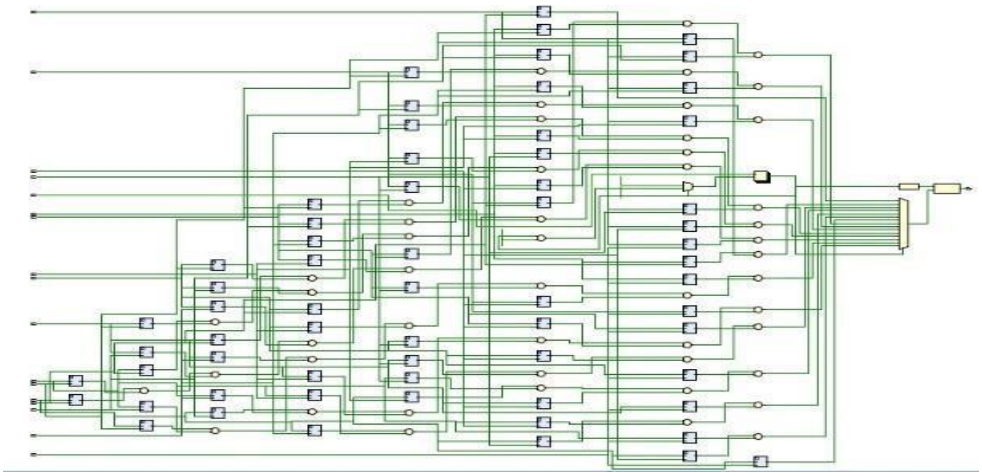


Fig.9. RTL Schematic of 8-tap FIR filter

IV. COMPARISONS

In this section we examine the different VLSI architectures of BW2 multiplier, BR4 multiplier and FIR filter with these two multiplier topologies.

```
================================================================
  Generated by:           Encounter(R) RTL Compiler RC14.25 - v14.20-s046_1
  Generated on:           Jul 28 2018  05:13:55 pm
  Module:                 baugh
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================

                  Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
----------------------------------------------------
baugh      136  7553.457 56700.749 64254.207
  f100       1    84.476   806.010   890.487
  f101       1    84.476   780.231   864.707
  f102       1    84.476   663.948   748.424
  f103       1    84.476   583.441   667.917
  f104       1    84.476   188.913   273.389
  f105       1    84.476   901.849   986.325
  f106       1    84.476  1086.454  1170.931
```

Fig.10.Dynamic power analysis of 8-bit BW2 multiplier

The dynamic power consumption of BW2 multiplier is shown in Fig.10. From above fig we observe that out of total 64254.2nW, the dynamic power of 56700.7nW and leakage power of 7553nW is consumed.

```
============================================================
  Generated by:           Encounter(R) RTL Compiler RC14.25 - v14.20-s046_1
  Generated on:           Jul 28 2018  05:28:06 pm
  Module:                 booth_4
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
------------------------------------------------
booth_4    260  7194.473 65994.905 73189.378
  f5        18  1365.656 12997.334 14362.990
    f16      3    88.570   865.701   954.270
    f1       1    86.962    52.242   139.204
    f2       1    86.962   194.894   281.856
    f3       1    86.962   251.193   338.155
```

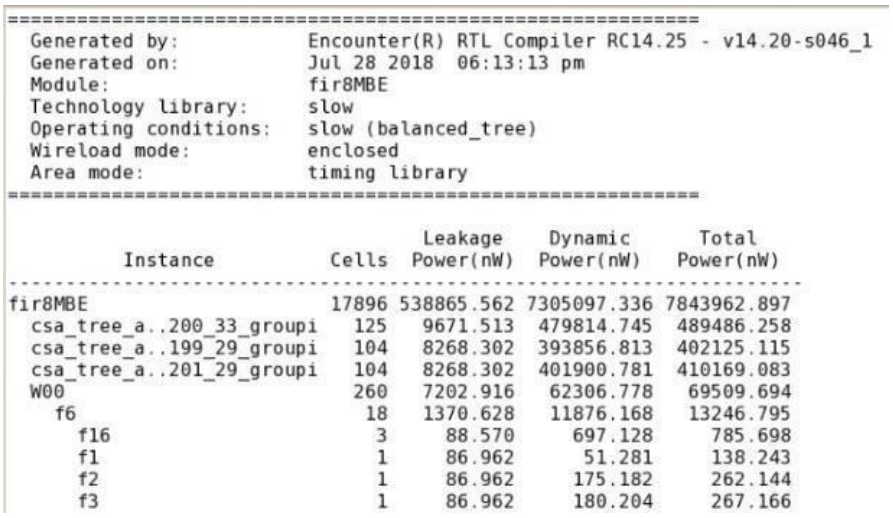
Fig.11. Dynamic power analysis of 8-bit BR4 multiplier

The dynamic power consumption of 8-bit BR4 multiplier is shown in Fig.11. From the above fig we observe that out of total 73189nW, the dynamic power of 65994nW and leakage power of 7194nW is consumed. Dynamic power reports of 8-tap FIR low pass filter using two multiplier topologies is shown below. The dynamic power report of implemented VLSI architecture for FIR filter using BW2 multiplier is shown in Fig.12. From the fig we observe that total of 7.55mW power the dynamic power of 6.59mW and leakage power of 0.71mW power is consumed.

```
============================================================
  Generated by:           Encounter(R) RTL Compiler RC14.25 - v14.20-s046_1
  Generated on:           Jul 28 2018  05:47:23 pm
  Module:                 fir8BAUGH
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                                    Leakage    Dynamic      Total
         Instance          Cells  Power(nW)  Power(nW)   Power(nW)
-------------------------------------------------------------------
fir8BAUGH                   9960 562395.376 6997528.133 7559923.509
  csa_tree_a..202_33_groupi  125   9650.847  478229.331  487880.178
  csa_tree_a..201_29_groupi  104   8268.302  391394.498  399662.800
  csa_tree_a..203_29_groupi  104   8268.302  398040.766  406309.068
  W00                        136   7570.892   55657.213   63228.105
    f100                       1     84.476     880.328     964.804
    f101                       1     84.476     682.761     767.237
    f102                       1     84.476     788.731     873.208
    f103                       1     84.476     497.779     582.255
    f104                       1     84.476      79.844     164.320
    f105                       1     84.476     998.621    1083.097
```

Fig.12. Dynamic power report of FIR filter using BW2 multiplier



```
====================================================================
  Generated by:           Encounter(R) RTL Compiler RC14.25 - v14.20-s046_1
  Generated on:           Jul 28 2018  06:13:13 pm
  Module:                 fir8MBE
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

                                       Leakage    Dynamic      Total
        Instance          Cells        Power(nW)  Power(nW)    Power(nW)
--------------------------------------------------------------------------
fir8MBE                   17896 538865.562 7305097.336 7843962.897
  csa_tree_a..200_33_groupi   125   9671.513  479814.745  489486.258
  csa_tree_a..199_29_groupi   104   8268.302  393856.813  402125.115
  csa_tree_a..201_29_groupi   104   8268.302  401900.781  410169.083
  W00                         260   7202.916   62306.778   69509.694
    f6                         18   1370.628   11876.168   13246.795
      f16                       3     88.570     697.128     785.698
      f1                        1     86.962      51.281     138.243
      f2                        1     86.962     175.182     262.144
      f3                        1     86.962     180.204     267.166
```

Fig.13. Dynamic power report of FIR filter using BR4 multiplier

The dynamic power report of implemented VLSI architecture for FIR filter using BR4 multiplier is shown in Fig.13. From the fig we observe that total of 7.84mW power the dynamic power of 7.3mW and leakage power of 0.53mW power is consumed.The dynamic power comparison results of multipliers and RFIR filter are shown below in Table.1.

S.NO	COMPONENT	DYNAMIC POWER (mW)
1.	Radix-4 Booth Recoded Multiplier	0.0659
2.	Radix-2 Baugh-Wooley Multiplier	0.0567
3.	FIR Filter with BR4 Multiplier	7.3050
4.	FIR Filter with BW2 Multiplier	6.9975

Table.1. Comparison results of multipliers

V. CONCLUSION

In this paper, dynamic switching power and area efficient reconfigurable FIR (RFIR) filter is implemented using the two most common topology multiplier techniques. In BW2 and BR4 multiplier topologies, carry save adder (CSA) and vector merging adder (VMA) are used. Performance comparisons results show that RFIR filter using BW2 multiplier has a less dynamic switching power when compared with RFIR filter using BR4 multiplier. In the future, the dynamic switching power can further be reduced RFIR filter by using KoggeStone Adder (KSA) in the two multiplier topologies.

.

REFERENCES

[1]. D. Blaauwet al., "IoT design space challenges: Circuits and systems, "in Symp. VLSI Technol. (VLSI-Technol.), Dig. Tech. Papers, Jun. 2014, pp. 1–2.

[2]. M. Mehendale, S. D. Sherlekar, and G. Venkatesh, "Low-power realization of FIR filters on programmable DSPs," IEEE Trans. Very LargeScale Integr. (VLSI) Syst., vol. 6, no. 4, pp. 546–553, Dec. 1998.

[3]. R. Hegde and N. R. Shanbhag, "A voltage overscaled low-power digital filter IC," IEEE J. Solid-State Circuits, vol. 39, no. 2, pp. 388–391, Feb. 2004.

[4]. B. Shim, S. R. Sridhara, and N. R. Shanbhag, "Reliable low-power digital signal processing via reduced precision redundancy," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 497–510, May 2004.

[5]. P. N. Whatmough, S. Das, D. M. Bull, and I. Darwazeh, "Circuit-level timing error tolerance for low-power DSP filters and transforms," IEEETrans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 6, pp. 989–999, Jun. 2013.

[6]. F. Sheikh, M. Miller, B. Richards, D. Markovi´c, and B. Nikoli´c, "A 1–190MSample/s 8–64 tap energy- efficient reconfigurable FIR filter for multi-mode wireless communication," in Proc. IEEE Symp. VLSI Circuits (VLSIC), Jun. 2010, pp. 207–208.

[7]. S. Y. Park and P. K. Meher, "Efficient FPGA and ASIC realizations of a DA-based reconfigurable FIR digital filter," IEEE Trans. CircuitsSyst. II, Exp. Briefs, vol. 61, no. 7, pp. 511–515, Jul. 2014.

[8]. P. Kulkarni, P. Gupta, and M. Ercegovac, "Trading accuracy for power with an underdesigned multiplier architecture," in Proc. 24th Int. Conf.VLSI Design, Jan. 2011, pp. 346–351.

[9]. K. Bhardwaj, P. S. Mane, and J. Henkel, "Power- and area-efficient approximate wallace tree multiplier for error-resilient systems," inProc. 15th Int. Symp. Quality Electron. Design (ISQED), Mar. 2014, pp. 263–269.

[10]. S. Hong, S. Kim, M. C. Papaefthymiou, and W. E. Stark, "Low power parallel multiplier design for DSP applications through coefficient optimization," in Proc. 12th Annu. IEEE Int. ASIC/SoC Conf., Sep. 1999, pp. 286–290.